Comparison of Truncated SVD and Jacobi-Davidson SVD within ESVDMOR

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Abstract

The reduction of parasitic linear subcircuits is one of many issues in model order reduction (MOR) for VLSI design. This issue is well explored, but the structure of these subcircuits has been changing recently. So far, the number of elements in these subcircuits was significantly larger than the number of connections to the whole circuit, the so called pins or terminals. This assumption is no longer valid in all cases. The simulation of these circuits requires new methods. In [1, 4, 5] the ESVDMOR algorithm is introduced as a way to handle this kind of circuits. Unfortunately, the ESVDMOR approach has some drawbacks because it uses the SVD for matrix factorization. We introduced the truncated SVD as an alternative to the SVD within the ESVDMOR [6]. In this paper we discuss the Jacobi-Davidson SVD approach [2,3] as another alternative matrix factorization method. We show the attributes, the advantages and disadvantages, and a runtime as well as an accuracy analysis of both methods.

References

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