Efficient algorithms for large resistor networks

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Electro Static Discharge (ESD) analysis is concerned with how fast electrical charge on the pins of a package can be discharged. Such information is important for the design of large-scale integrated circuits, since the functional operation of chips can easily be affected or destroyed by peak charges (caused, for instance, by a human touch).

The discharge usually takes place through the power network and substrate. Both the power network and the substrate are resistive. The discharge paths are modeled by very large resistance networks connected through diodes: the networks can contain up to millions of nodes and resistors.

In practical ESD analysis, one is interested in fast solutions for three related problems:

1. Computation of path resistances between external nodes. The number of external nodes can vary from $O(1)$ to $O(10^4)$.

2. Reduction of resistor networks, keeping selected external nodes. The number of external nodes can vary from $O(1)$ to $O(10^4)$. The reduced network should be sparse, so that it can simulated efficiently together with other parts of the system.

3. Computation of current densities in resistors. Here one needs to know whether the metal interconnect is thick enough for the amount of current. The number of resistors varies from $O(10^5)$ to $O(10^6)$.

We will present efficient numerical algorithms for the solution of these problems. Numerical experiments with real-life networks show that our algorithms are factors faster than commercial software while preserving accuracy.