ON SYNTHESIS OF REDUCED ORDER MODELS

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Several synthesis procedures for realizing reduced mathematical models into RLC circuits are presented. The approaches are compared in terms of: quality of approximation, preservation of structure and sparsity and applicability to Multi-Input-Multi-Output systems.

1. Introduction. An emerging problem in simulation of VLSI circuits is that of model reduction for the interconnect. Advanced passivity preserving reduction methods have been developed, which reduce the dynamical system of an original circuit to an approximate mathematical model of smaller dimension. Passivity ensures that the reduced mathematical model can be synthesized into an RLC netlist [1], which is used in place of the original circuit during simulation. This survey compares several synthesis methods for realizing reduced SISO and MIMO systems into RLC circuits.

2. Problem description. The reduced circuit model obtained after synthesis should be both "small" and "sparse" (i.e. generate fewer unknowns *and* contain fewer circuit elements than the original circuit). This would ensure that the reduced circuit is indeed cheaper to simulate that the original one. The location of the input and output nodes have to be preserved in addition. It turns out that, while SISO realizations are achieved rather easily, MIMO systems are difficult to synthesize when low-dimensionality, accuracy, sparsity and input-output structure preservation should be achieved simultaneously. This is shown in the following preliminary results.

A Single-Input-Single-Output RLC circuit resulting from the parasitic extraction of a spiral inductor is reduced and synthesized with the SAPOR/IOPOR [2], [3] structure preserving approach. The number of circuit elements was reduced from 39 to 9, and the Pstar[1] simulations of the original and reduced synthesized circuits matched closely.

Table 2.1
Resistive network: synthesis summary

System	Non-zeros	Resistors	States	Inputs/Outputs
Original	9666	3683	2299	59
Reduced	9690	3583	114	59

Next, reduction of a Multi-Input-Multi-Output resistive network was attempted with the same approach, while the input-output structure is preserved. Table 2.1 shows that although the system dimension is reduced from 2299 to 114, the reduced netlist is "dense" and still has a very large number of resistors (3583 vs. originally 3683). It is still an open question, whether in the end the simulation time is determined by the number of unknowns, the number of elements or the sparsity of the synthesized model. This study aims at understanding these effects via several examples. For future work, sparse Krylov projections will be investigated, with the goal of preserving low dimensionality, sparsity, and input-output structure simultaneously. Comparisons with the Foster realization [4] approach will also be presented.

*Marie Currie fellow as part of the COMSON project Contract Number MRTN-CT-2005-019417 at TU/Eindhoven and NXP Semiconductors, Eindhoven, the Netherlands.

[1]In-house analog circuit simulator of NXP Semiconductors.

REFERENCES

[1] A. C. Antoulas, *Approximation of Large-Scale Dynamical Systems.* Philadelphia, PA: SIAM, 2005.

[2] F. Yang, X. Zeng, Y. Su, and D. Zhou, “Rlc equivalent circuit synthesis method for structure-preserved reduced-order model of interconnect in vlsi,” *Commun. Comput. Phys*, vol. 3, no. 2, pp. 376–396, February 2008.

[3] R. Freund, “Sprim: Structure-preserving reduced-order interconnect macromodeling,” in *Proc. IEEE/ACM Int. Conf. on Coputer Aided Design (ICAAD'04)*, Los Alamitos, CA, 2004, pp. 80–87.

[4] E. A. Guillemin, *Synthesis of passive networks*, 2nd ed. John Wiley, 1959.