Universität Hamburg
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Fakultät für Mathematik, Informatik
und Naturwissenschaften
Fachbereich Mathematik

Lothar-Collatz-Kolloquium über Angewandte Mathematik

Donnerstag, den 27. November 2025, um 14:30 Uhr, im Hörsaal 6

Prof. Dr. Vadym Aizinger*
(Universität Bayreuth, Fakultät für Mathematik, Physik und Informatik, LS für Wiss. Rechnen)

Performance portability of a discontinuous Galerkin shallow water model on CPUs, GPUs, and FPGAs

Zusammenfassung/Abstract:

The increasing heterogeneity of available hardware architectures have made numerical modeling, particularly for high-performance computing (HPC), increasingly dependent on portability across diverse computing platforms. Beyond functional portability -- ensuring that models can be compiled and executed on all supported hardware --- performance portability is crucial for maximizing efficiency on current and future HPC hardware. Numerical model codes building upon performance portable approaches can thus leverage emerging hardware trends and sustain high computational performance across evolving architectures. Since the requirements for an efficient numerical code differ greatly between e.g. CPUs and GPUs, approaches focusing on the program code alone lead to limited improvements and often produce an unreadable model code. Our work focuses on integrating numerical, algorithmic, and computational approaches to achieve computational performance and performance portability. This concept is illustrated using our SYCL implementation of a discontinuous Galerkin method for the 2D shallow water equations which achieves portability across a broad spectrum of hardware platforms---including CPUs, GPUs, and FPGAs. SYCL adheres to the separation-of-concerns principle by translating standard C++ code into hardware-optimized binaries via vendor- or third-party-provided backends. Using a suitable programming style and targeted data type optimizations, we demonstrate that our single-source code delivers excellent performance across all supported hardware platforms.

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